

Invalidation Search Sample in Chinese Language

Contents

- 1 ?????????CLIP???????FET?????
 - ◆ 1.1 ??????????
 - ◇ 1.1.1 ????
 - ◇ 1.1.2 ????
 - ◆ 1.2 ??????????(CLIP ??????)
 - ◇ 1.2.1 ??????CLIP ??????
 - ◇ 1.2.2 ????
 - ◇ 1.2.3 ????
 - ◇ 1.2.4 ????
 - ◇ 1.2.5 ????
 - ◇ 1.2.6 ????
 - ◇ 1.2.7 ????
 - ◆ 1.3 ????
 - ◇ 1.3.1 ??CLIP??
 - ◇ 1.3.2 ???CLIP???
- 2 ????????
- 3 ????
 - ◆ 3.1 ????
 - ◆ 3.2 ????
 - ◇ 3.2.1 ????
 - ◇ 3.2.2 ????
- 4 ???????
 - ◆ 4.1 ??1
 - ◆ 4.2 ?? 2
 - ◆ 4.3 ????
 - ◆ 4.4 ??

?????????CLIP???????FET?????

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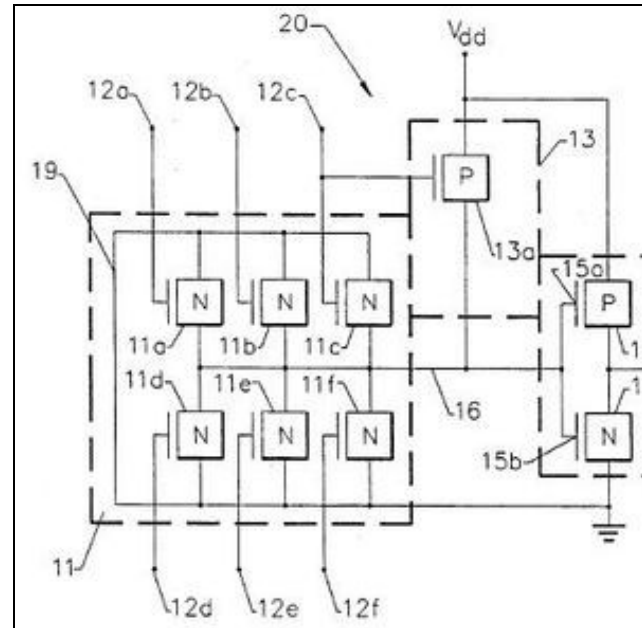
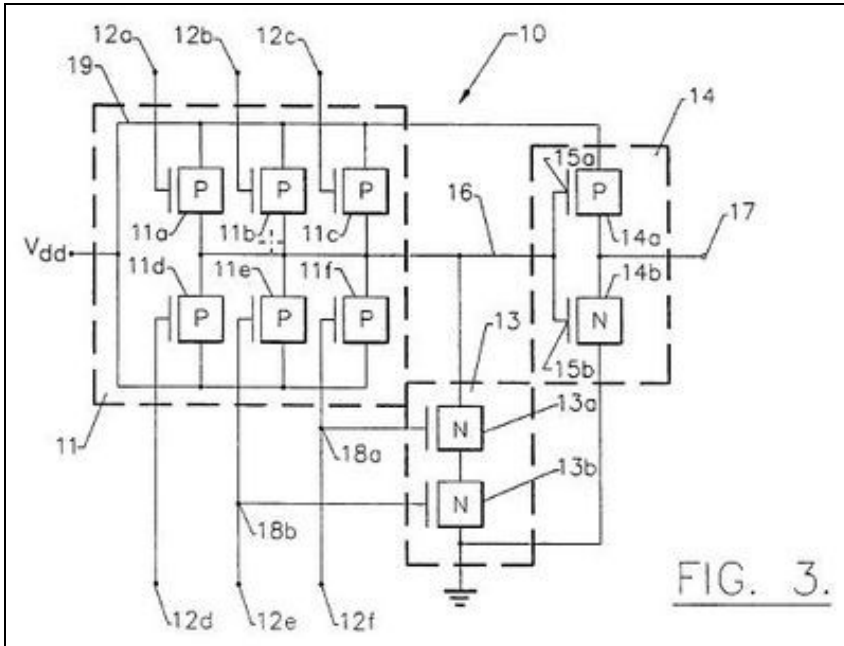
- ???CMOS??

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- ?????????????????CMOS??MOS????????????????????????????????????MOS????
- ?????????????????FET????????????????FET??

?????????????(CLIP ??????)

?????CLIP ??????



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- ??????????CLIP?FET?????????????????????????????
- ???FET????????????????????????????????CLIP?????????
- ?????????????????????????????

- ?????????12a-12e????????17?????
- ?????????????FET21????FET13????????12a-12f????14????????Vdd????????FET21????FET13????

- ?????CLIP????????12a-12e????????FET23????????14???17?????
- ???CLIP???
 - ◆ ?????14???17????FET23a???24a?
 - ◆ ?????????????12a-12f????????????11a-11e????14???17????Vdd????????FET21?23????????17???????????

- ??X?Y????

- ??? - Micropat

S.No	Scope	Concept	Query	Hits
1	Claims, Title or Abstract	P or N channel FET?s used to increase the speed, minimize the capacitance, minimize delay time	Query - ((p or n) adj2 (channel or type) NEAR (FET or (field adj1 effect adj1 transistor*))) AND (((increase or step adj1 up or increment or high) NEAR (speed or performance)) OR ((minimize* or reduc* or lower* or (cut adj1 down)) NEAR capacitance) OR ((minimize* or reduc* or lower* or (cut adj1 down)) NEAR delay)) Priority Date (earliest): <19910131	134
2	Claims, Title or Abstract	Increase the speed of the logic circuits that includes transistors	Query - (increase or step adj1 up or increment or high OR enhanc*) SAME ((logic adj1 (circuit or gate or stage)) AND ((p or n) adj2 (channel or type) NEAR (transistor or *FET*1 or (field adj1 effect adj1 transistor*))) Priority Date (earliest): <19910131	32
3	Claims, Title or Abstract	FET?s connected in parallel with the drains connected to Vdd	Query - ((p or n) adj2 (channel or type) NEAR (FET*1 or (field adj1 effect adj1 transistor*))) WITH parallel WITH (Vdd or potential or supply) Priority Date (earliest): <19910131	58
4	Full patent spec.	FET?s connected in parallel to increase the speed	Query: ((p or n) adj2 (channel or type) NEAR (FET*1 or (field adj1 effect adj1 transistor*))) WITH parallel WITH (Vdd or potential or supply) AND (logic adj1 (circuit or gate)) AND (((increase or step adj1 up or increment or high) NEAR (speed or performance)) OR ((minimize* or reduc* or lower* or (cut adj1 down)) NEAR capacitance) OR ((minimize* or reduc* or lower* or (cut adj1 down)) NEAR delay)) Priority Date (earliest): <19910131	33
5	Full patent spec.	FET Connection having common output	Query - ((p or n) adj2 (channel or type) NEAR (*FET*1 or (field adj1 effect adj1 transistor*))) SAME (parallel and (Vdd or potential or supply) and (common adj1 output)) Priority Date (earliest): <19910131	22
6	Full patent spec.	FET?s with channel width, channel lengths and saturation current described	Query: (channel adj1 (width and length)) and (saturation adj1 current) and ((p or n) adj2 (channel or type) NEAR (FET*1 or (field adj1 effect adj1 transistor*))) Priority Date (earliest): <19910131	13
7	Full patent spec.	FET?s of gating stage connected serially to common output and ground	Query: ((p or n) adj2 (channel or type) NEAR (FET*1 or (field adj1 effect adj1 transistor*))) WITH (((serial or serially) NEAR2 (connected or connection)) and (ground or VSS or potential)) Priority Date (earliest): <19910131	98
8	Claims	Increasing the speed in the logic circuits	Query - (increase or step adj1 up or increment or high) WITH (logic adj1 (circuit or gate)) AND (transistor or FET*1 or (field effect transistor*)) and speed Priority Date (earliest): <19910131	100
9	Full patent spec.	Common diffusion to minimize the internal capacitance	Query: ((common or shared or mutual) WITH diffusion) and ((minimize* or reduc* or lower* or (cut adj1 down)) NEAR capacitance) AND (FET or (field adj1 effect adj1 transistor*) or transistor) Priority Date (earliest): <19910131	48
10	Full patent spec.	Increasing the carrier mobility in P-channel FET?s by doping germanium	Query - (p adj2 (channel or type) NEAR (transistor or *FET*1 or (field adj1 effect adj1 transistor*))) AND (((increase or step adj1 up or increment or high or enhanc* or equalize) NEAR (carrier NEAR mobilit*)) AND germanium Priority Date (earliest): <19910131	12
11	Total		1 OR 2 OR 3 OR 4 OR 5 OR 6 OR 7 OR 8 OR 9	542

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- ??? - Google scholar that covers IEEE
 - ◆ ???? - 1985-1990

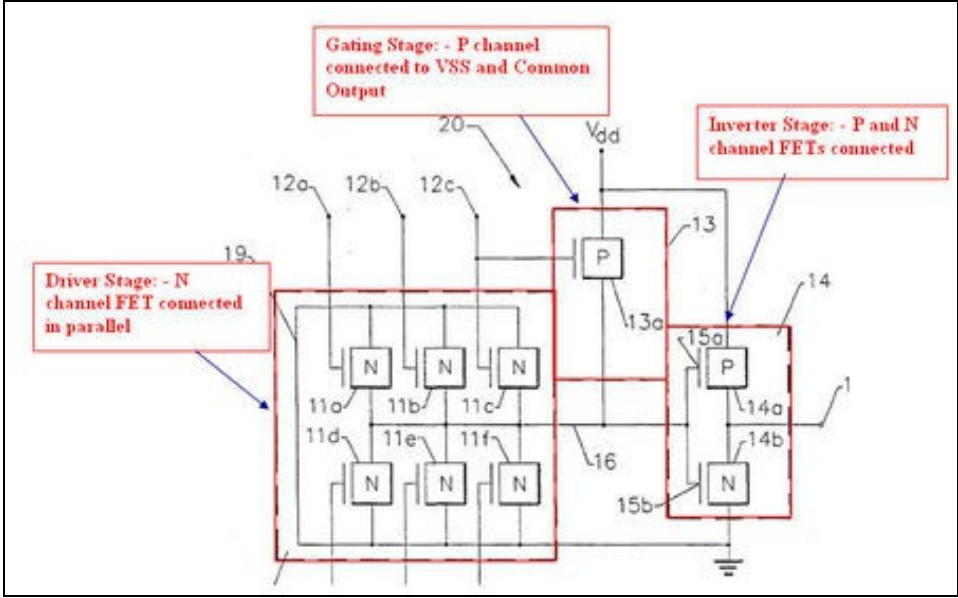
S.no	Query	Hits
1	P N channel FET logic increase OR enhance OR high "speed"	399
2	P channel FET logic speed increase OR enhance OR high "germanium"	52
3	FET logic parallel speed drain increase OR enhance OR high OR Vdd OR potential -patents	267
4	FET logic parallel speed increase OR enhance OR high OR Vdd OR potential "common output"	30
5	P N channel FET logic speed inverter OR complimentary "common output"	4
6	P-channel N-channel FET common diffusion "parallel"	114
7	P-channel N-channel FET germanium increase OR enhance OR high "carrier mobility"	9
8	P-channel N-channel FET germanium increase OR enhance OR high "carrier mobilities"	3
9	P-channel N-channel FET germanium increase OR enhance OR high "saturation current"	6
10	P-channel N-channel FET minimize OR decrease OR reduce "internal capacitance"	4
11	Total	888

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- ?BYTE?????????????
 - ◆ Gallium Arsenide Chips - Volume 9, issue 12 (November, 1984)

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NAME	CLIP FET	
FIGURE		
	Gating Stage: - P channel connected to VSS and Common Output	Inverter Stage: - P and N channel FETs connected
TYPE	Patent:- US5247212	IEEE JOURNAL C
Title	Complementary logic input parallel (CLIP) logic circuit family	A 15-ns CMOS 64
Assignee	THUNDERBIRD TECH INC (US)	STANLEY E. SCH L. FRANCH, PAUL PETER W. COOK WILLIAM F. POKO
IPC		

